2018 IEEE S3S Conference

October 15 – 18, 2018, Hyatt Regency San Francisco Airport

s3sconference.org

IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference

Overview: This conference has grown over the past several decades to deliver a wealth of important information on the most relevant and state-of-the-art technology topics including 3D Integration, Ultra Low Power Circuits and Devices, and Silicon on Insulator Technology. Recently the IEEE S3S Conference has been a hot spot for the latest research on 3D Integration to enable another dimension of scaling. Even more recently, the conference has been a place where the newest results on Ultra-Low Power Circuits are discussed and shared. The IEEE S3S Conference is not only a venue where the industry and academia publish their latest works but also a place where colleagues come together to have meaningful informal discussions. We also have instructional short courses and tutorials on the most exciting and new technology topics.

Important Dates

Paper Submission Deadline: May 21, 2018

Acceptance Notification: July 1, 2018

Scope: We welcome papers in the following areas:

Silicon on Insulator (SOI) Technology

- Fully Depleted Silicon on Insulator Technology
- Advanced Materials, Substrate and Processes
- Device Physics, Characterization and Modelling
- Sensors, MEMS, BioMEMS
- Non-Digital Devices and Applications (RF, High-Voltage, Photonics, Analog…)
- Novel SOI Structures, Circuits and Applications
- SOI Design, Circuits and Applications

Low-Voltage Devices

- Low-Dimensional (1D, 2D) Transistors
- Tunnel FETs
- Negative Capacitance FETs
- Piezoelectric FETs
- Nano-Electromechanical Switches
- Low Voltage Memory Technologies
- Metal-Insulator Transitional Devices
- Spintronic Devices

Low-Power Circuits

- Low-Power and Ultra-Low-Power Digital circuits
- Energy efficient designs and methodologies
- Power management techniques
- Asynchronous Circuits
- Energy Harvesting solutions
- Low power, reliable and resilient solutions
- Analog/mixed-signal circuits for wireless communications
- Innovative ICs
- Near threshold and sub-threshold designs
- Low power applications: IoT, Automotive, Data mining …

3D Integration

- System in Package
- Through Silicon Via (TSV) Technology
- 3D System Integration
- Fabrication Techniques and Bonding Methods
- Design and Test Methodologies
- Processes for Multi Wafer Stacking
- 3D IC EDA and Design Technology
- Heterogeneous Structures
- 3D Manufacturing and Logistics
- Reliability of 3D Circuits
- Fault Tolerant 3D Designs

Paper Submission

Prospective authors should prepare a 2-page abstract (guidelines at s3sconference.org/preparation-of-abstracts/). Acceptance is based on paper's technical quality and relevance.

General Chair: Ali Khakifirooz, Intel

Technical Program Chair: Bruce Doris, IBM

Conference Manager Contact

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