2017 IEEE S3S Conference

IEEE International SOI-3D-Subthreshold Microelectronics Technology Unified Conference
16 - 19 October 2017
Hyatt Regency, San Francisco Airport, 1333 Burlingame, CA
s3sconference.org

Now in its 43rd year, this conference is bringing industry leaders and academic experts to discuss their latest research and technology development achievements. Our contributed papers and invited talks are mainly focused on SOI technology, low-voltage devices/circuits/architectures, and 3D integration. These three technologies will play a major role in tomorrow's industry as they enable application-tailored and energy/cost efficient circuit designs.

Plenary Speakers:

Monday, October 16, 8:00 - 10:00 AM

Al Fazio, Senior Fellow, Intel, "3D NAND and 3D XPoint™: 3D Non-Volatile Memories Ushering in a New Era in Scaling, Performance and Applications."
Ted Letavic, Senior Fellow, GLOBALFOUNDRIES, "Ultra-low Power Semiconductor Platform Solutions for Intelligent Compute and Connect."
Suman Datta, Chang Family Professor of Engineering Innovation, University of Notre Dame, "In Quest of the Next Information Processing Platform."

Rump Session: Semiconductor Technologies Driving Architectures for Brain-Like AI

Monday, October 16, 8:00 - 10:00 PM
Moderator: Ali Keshavarzi, Leading Edge Research, LLC

William Chappell, Director, DARPA MTO
Suman Datta, Professor, University of Norte Dame
Wilfried Haensch, Manager, IBM T.J. Watson Research Center
Norm Jouppi, Distinguished Engineer, Google
Amir Khosrowshahi, CTO, AI Products Group, Intel
Dinesh Maheshwari, Partner, Silicon Catalyst
Kaushik Roy, Professor, Purdue University

AI is enabling a variety of applications such as voice and image recognition cost-effectively with low power. As such it is receiving a wide range of attention in public. AI is highly debated among technical communities while commercial companies are rushing for business opportunities. Semiconductor materials, devices, integration techniques and technologies are being probed to enable architectures for AI systems and applications.
Silicon-based semiconductor technology has driven efficient compute per watt for example in the case of application processors utilizing advanced technology nodes with established von Neumann architecture in pervasive mobile devices. Energy-efficient computing measured in MIPS/W is paramount for AI and for the future. The key question is: What drives MIPS/W to achieve efficiency in the range of human brain? What semiconductor technologies will guide architectures behind brain-like energy-efficient computing that is required for AI?
A panel of experts will be discussing and debating various technical directions and market opportunities while exploring various approaches. Technical topics span the range of materials/processes/devices/circuits/integration schemes that are driving architectures toward establishing power efficient AI.

This year's Rump Session is open to all IEEE members.

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FDSOI Design Shortcourse

Thursday, October 19

This full-day shortcourse brings experts from the academia and industry to teach different aspects of circuit design in FDSOI. Given the FDSOI technology offering at multiple foundries and multiple nodes, including 65nm, 28nm and 22nm, we believe this is a unique opportunity for circuit designers to learn first-hand from distinguished experts and bring in their questions and concerns. In addition to the following lectures, EDA vendors, IP vendors and foundry technologists will be available for in-depth discussions during break-outs and poster session.

Course Organizer: Philippe Flatresse, STMicroelectronics

Fundamentals of FDSOI Design, Yoshiki Yamamoto, Renesas
Body Biasing Techniques and Body Bias Generators, Andreas Burg, EPFL
FDSOI Platforms and Applications, Jeff Cunningham, NXP Semiconductors
Physical Implementation of Low Power SoC Chip in SEC 28nm FD-SOI, Jiong Zhu, Verisilicon
Ultra-Low Voltage and Ultra-Low Power Designs for IoT, Sebastien Thuries, CEA Leti
High Speed Analog Design, Yusuf Lebleblici, EPFL
Analog and RF Design in FDSOI, Carlo Tinella, Asygn
RF Design in FDSOI, Baudouin Martineau, CEA Leti

3D Technology Tutorial

Tuesday, October 17, 2:20 - 5:20 PM

Three dimensional chips stacked using Through Silicon Via (TSV) technology has been under consideration and the subject of intensive research for several years now. This tutorial covers the technology, applications, design and CAD for 3DIC. The technology will be introduced, including TSVs, face to face technologies, integration options and interposers. Applications will be discussed as driven by cost, performance and power efficiency needs. Examples will be given from the commercial world and the author's own research. CAD and CAD-driven design will be covered including verification, test, and thermal evaluation.
Paul Franzon, North Carolina State University
Zvi Or-Bach, MonolithIC 3D™ Inc.

Special Session on Neuromorphic Computing

Wednesday, October 18, 8:00 AM - 12:20 PM

As Dennard scaling is approaching its limits, a new computing paradigm involving system, circuit and technology co-innovation is on demand. The "Brain-like" computation, a.k.a. the neuromorphic computing has been considered as the most promising candidate as a replacement or supplement to existing Van Neumann computers. Both emerging semiconductor devices and circuit/system designs have been studied extensively and many progress has been achieved in recent years.

Session Organizer: Nuo Xu, Samsung

Philip H.-S. Wong, Stanford University
Shimeng Yu, Arizona State University
Giacomo Indiveri, ETH Zurich
John Arthur, IBM Research, Almaden
Arvind Kumar, IBM T.J. Watson Research Center
Zhe Wan, UCLA
Zhengya Zhang, University of Michigan, Ann Arbor