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Technical Program

2017 Selected and Invited Papers covering a wide range of topics in the areas of SOI, 3D Integration and low-voltage, devices, circuits and architectures

PAG. 18

Educational Opportunities

23rd Annual Short Course: *FDSOI. Everything you always wanted to know about FDSOI*
3D Tutorial: *Covering technology, applications, design and CAD for 3DIC*

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Registration Information

Everything you need to know about registering for the 2017 IEEE S3S Conference

2017
IEEE S3S Conference
ADVANCE PROGRAM

IEEE SOI-3D-SUBTHRESHOLD MICROELECTRONICS TECHNOLOGY UNIFIED CONFERENCE

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IEEE S3S CONFERENCE
6930 De Celis Place, #36, Van Nuys, CA 91046
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General Chair's Message

The organizing committee and I are pleased to invite you to attend the 2017 IEEE S3S Conference to be held on October 16th through 19th, 2017 at the Hyatt Regency San Francisco Airport hotel.

The past year has seen a continuous growth in the interest for low-power electronics and communications. The three technologies at the heart of the IEEE SOI – 3DI – Subthreshold (S3S) Microelectronics Technology Unified Conference's program will help bring to the consumer market, applications as diverse as mmWave transmissions, energy harvesting and energy efficient computing, in a budget-constrained industry.

This year we will gather once again in the very conveniently located Hyatt Regency San Francisco Airport hotel to discuss the upcoming trends of our field.

On Monday October 16th, we will get the point of view of some of our industry leaders during the Plenary Session. Al Fazio, Intel Senior Fellow and Director of Memory Technology Development will discuss the advances made in 3D memories, covering both 3D NAND and 3D XPoint technologies, Geoff Lees, General Manager of the Microcontroller group at NXP Semiconductors will present recent developments and future directions in MCUs, and Ted Letavic, GlobalFoundries's Senior Fellow, will discuss the company's advancement in FDSOI, RFSOI and photonics technologies.

We will also explore and discuss exciting future computer architectures and applications and how the three pillars of our conference will contribute to those through a rump session on AI, deep learning and neuromorphic computing on Monday evening and two dedicated sessions on Wednesday October 18th.

A full-day shortcourse on FDSOI circuit design will be held on Thursday October 19th, and along with several sessions dedicated to FDSOI circuits, it provides a unique opportunity for circuit designers interested in the technology.

The 3DI part of our program also keeps growing, and the conference will host 5 sessions dealing with various aspects of this growing field. We will also have a 3D tutorial on Tuesday 10/17 afternoon. A satellite workshop organized by Leti and Qualcomm on CoolCube™/3DVLSI open Workshop will complement our program. The workshop is dedicated to High Density 3D-IC Technologies including Monolithic 3D Integration (called CoolCube™ Technology at Leti). The extended CoolCube™ project's goals include building a complete ecosystem that takes the technology from design to fabrication. Registration is free and available to S3S attendees. However, since seating is limited, registration is by invitation only. If interested, please send an email to jean-eric.michallet@cea.fr.

We will also have two poster sessions this year. The first one will take place in the evening of Monday 10/16, and will give us the opportunity to discuss presenters' work in more details, during a friendly reception.
The second will host posters presented by students participating in the E3S program and will be a preview of the 5th Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistor Workshop, which will take place October 19-20 at the campus of the University of California, Berkeley. The goal of this event is to bring together researchers in academia, industry, and national labs from around the world working on breakthroughs in next generation low-energy information processing systems.

Together with the satellite events organized by our partners and colleagues, the 2017 edition of the S3S conference will present an even better opportunity than the previous one to gather a broad picture of the quickly developing trends and technology that will shape tomorrow's semiconductor industry.

Our numerous social events in a friendly setting will further provide opportunities to discuss those trends and exchange point of views. Do not miss the Wednesday evening networking reception!

I am looking forward to fruitful discussions with you all during the conference. Your presence is of course key to the event's success, as are the high-quality contributions of all presenters, to which I extend my thanks.

Finally, I thank the organizing committee and the conference manager, for their hard work and for making the conference happen every year.

Fred Allibert
2017 General Chair

CONFERENCE AT-A-GLANCE

	MONDAY October 16, 2017		TUESDAY October 17, 2017			WEDNESDAY October 18, 2017		THURSDAY October 19, 2017
7:00AM	Breakfast		Breakfast			Breakfast		Breakfast
8:00AM	Session 1: Plenary Speakers		Session 9: RF Circuits	Session 10: Embedded Memories	COOLCUBE™/3DVLSI OPEN WORKSHOP Limited Seating Reserve Early	Session 17: Neuromorphic Computing 1	Session 18: Monolithic 3D 2	FDSOI Short Course
10:00AM	Break		Break			Break		Coffee Break / Discussion
10:20AM	Session 2: Technology Directions and Ecosystem	Session 3: FDSOI Circuits 1	Session 11: SOI Wafers	Session 12: Low Power Circuits 1		Session 19: Neuromorphic Computing 2	Session 20: Heterogeneous Integration	FDSOI Short Course
12:20PM	Lunch (on own)		Lunch (on own)			Lunch (on own)		Lunch
1:20PM 2:20PM	Session 4: Advanced SOI Devices 1	Session 5: Monolithic 3D 1	Session 13: Advanced SOI Devices 2	Session 14: Low Power Circuits 2		Session 21: FDSOI Circuits 2	Session 22: Precise Wafer Bonding	FDSOI Short Course
3:20PM	Break		Break			Break		Coffee Break / Poster Session
3:40PM	Session 6: Modeling and Charaterization	Session 7: 3D Wafer Stacking	Session 15: Advanced SOI Technology	Session 16: Low Voltage Devices 1		Session 23: Low Voltage Device 2	Session 24: Monolithic 3D 3	FDSOI Short Course
						Awards and Closing Remarks		
6:00PM	Session 8: Poster Session and Reception		E3S Poster Session and Reception			Networking Reception		
8:00PM	Rump Session		Cookout					

MONDAY OCTOBER 16, 2017

7:00AM CONTINENTAL BREAKFAST

8:00AM SESSION 1: PLENARY SPEAKERS

1.1 **3D NAND and 3D XPoint™: 3D Non-Volatile Memories Ushering in a New Era in Scaling, Performance and Applications**
Al Fazio; *Senior Fellow at Intel*

1.2 **Ultra-low Power Semiconductor Platform Solutions for Intelligent Compute and Connect**
Ted Letavic; *Senior Fellow, GLOBALFOUNDRIES*

10:00AM BREAK

10:20AM SESSION 2: TECHNOLOGY DIRECTIONS AND ECOSYSTEM

2.1 **Scaling the Compute and High Speed Networking Needs of the Data Center with Silicon Photonics**
Robert Blum; *Intel, Santa Clara, CA, USA (Invited Speaker)*

2.2 **Realizing the Next Growth Wave for Semiconductors and MEMs – A New Approach to Enable Innovative Startups**
D. Armbrust, R. Lazansky, N. Kepler and R. Goldman; *Silicon Catalyst, San Jose, CA, USA (Invited Speaker)*

2.3 **Why FD SOI and SOI are Important within the Global Electronic Industry**
Handel Jones; *IBS, Los Gatos, CA, USA (Invited Speaker)*

SESSION 3: FDSOI CIRCUITS 1

3.1 **Ultra Low Energy Cryptographic Engine Designs and SOTB Chip Fabrication Services in Japan**
Makoto Ikeda, *Department of Electrical Engineering and Information University of Tokyo, Bunkyō, Tokyo, Japan (Invited Paper)*

3.2 **An Implementation of 2RW Dual-Port SRAM Using 65 nm Silicon-on-Thin-Box (SOTB) for Smart IoT**
Y. Yamamoto[1], T. Hasegawa[1], M. Yabuuchi[1], K. Nii[1], Y. Sawada[1], S. Tanaka[1], Y. Shinozaki[2], K. Ito[2], H. Shinkawata[1] and S. Kamohara[1]; [1]Renesas Electronics Corporation, *Tokyo, Japan,* [2]*Nippon Systemware Co. Ltd., Tokyo, Japan*

3.3 **Power and Performance Comparision of Body Bias in 28HPC and Back Bias in 22FDX**
K. Zhao, J. Wang, j. Li, B. Yang, H. Wang, M. Shen, F. Yu, L. Xu; *Shanghai Fudan Microelectronics Group Company Limited, Shanghai, China*

3.4 **Level-Shifter Free Approach for Multi-VDD SOTB Employing Adaptive Vt Modulation for pMOSFET**
K. Usami[1], S. Kogure[1], Y. Yoshida[1], R. Magasaki[1] and H. Amano[2]; [1]*Shibaura Institute of Technology, Koto-ku, Tokyo, Japan,* [2]*Keio University, Kouhoku-ku, Yokohama, Japan*

12:20PM **LUNCH** *(ON OWN)*

1:20PM **SESSION 4: ADVANCED SOI DEVICES 1**

4.1 **FinFETs on Insulator with Silicided Source/Drain**
H. Zhu, L. Jun, Q. Zhang, H. Yin, H. Zhong, C. Zhao; *Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences and the University of Chinese Academy of Sciences, Beijing, China (Invited Speaker)*

4.2 **First Demonstration of Symmetric Lateral NPN Transistors on SOI Featuring Epitaxially-Grown Emitter/Collector Regions**
P. Hashemi, J.-B. Yau, K. K. Chan, T. H. Ning and G. G. Shahidi; *IBM Research Thomas J. Watson Research Center, Yorktown Heights, New York, USA*

4.3 **Gate Controlled Diode Characteristics of Super Steep Subthreshold Slope PN-Body Tied SOI-FET for High Efficiency RF Energy Harvesting**
S. Momose[1], J. Ida[1], T. Mori[1], T. Yoshida[1], J. Iwata[1], T. Horii[1], T. Furuta[1], K. Itoh[1], K. Ishibashi[2], and Y. Arai[3]; *[1]Division of Electrical Engineering, Kanazawa Institute of Technology, Ishikawa, Japan, [2]The University of Electro-Communications, Tokyo, Japan, [3]High Energy Accelerator Research Org. KEK, Tsukuba, Japan*

4.4 **A Novel Photodetector Based on the Interface Coupling Effect in Silicon-on-Insulator MOSFETs**
JN. Deng[1], JH. Shao[1], BR. Lu[1], YF. Chen[1], A. Zaslavsky[2], S. Cristoloveanu[3], M. Bawedin[3] and J. Wan[1]; *[1]State Key lab of ASICs and Systems, School of Information Science and Engineering, Fudan University, Shanghai, China, [2]Department of Physics and School of Engineering, Brown University, Providence, Rhode Island, USA, [3]IMEP-LAHC, INP-Grenoble/Minatec, Grenoble, France*

SESSION 5: MONOLITHIC 3D 1

5.1 **3D Nanomagnetic Logic: How Far Beyond CMOS?**
M. Becherer[1], G. Csaba[2], G. Žiemys[3]; *[1]Nanoelectronics Technical University Munich, Munich, Germany, [2]Pazmany Peter Catholic University, Budapest, Hungary, [3]Technical Electronics Technical University Munich, Munich Germany (Invited Speaker)*

5.2 **Vertically-Composed Fine-Grained 3D CMOS**
M. Li[1], J. Shi[1], M. Rahman[2], S. Khasanvis[3], S. Bhat[1], C. A. Moritz[1]; *[1]Electrical and Computer Engineering, University of Massachusetts, USA, [2]Computer Science and Electrical Engineering, University of Missouri, USA, [3]BlueRISC Inc. USA (Invited Speaker)*

5.3 **Double-Gate Si Junction-less n-Type Transistor for High Performance Cu-BEOL Compatible Applications Using 3D Sequential Integration**
A. Vandooren, L. Witters, E. Vecchio, E. Kunnen, G. Hellings, L. Peng, F. Inoue, W. Li, N. Waldron, D. Mocuta, N. Collaert; *IMEC, Leuven, Belgium*

5.4 **Cost Projections and Benefits for Transistor-Level 3-D Integration with Stacked Nanowires**
N. K. Macha, M. Rahman; *Department of Computer Science & Electrical Engineering, University of Missouri Kansas City, Missouri, USA*

3:20PM **BREAK**

3:40PM **SESSION 6: MODELING AND CHARACTERIZATION**

6.1 **Investigations on Contact Punch-Through in 28 nm FDSOI through Virtual Fabrication**
B. Vianne[1], P. Morin[1], C. Beylier[1], J.-C. Giraudin[1], S. Desmoulins[1], R. Gonella[1], A. Juncker[2], D. Fried[2]; *[1]STMicroelectronics, Crolles, France, [2]Coventor, Inc, Massachusetts, USA*

6.2 **New Method for Individual Electrical Characterization of Stacked SOI Nanowire MOSFETs**
B. C. Paz[1], M. Cassé[2], S. Barraud[2], G. Reimbold[2], M. Vinet[2], O. Faynot[2] and M. A. Pavanello[1]; *[1]Centro Universitário FEI, São Bernardo do Campo, Brazil, [2]CEA, LETI, MINATEC Campus, Grenoble, France*

6.3 **Advanced Characterization Technique for the Extraction of Intrinsic Effective Mobility in Ultra-Thin-Body Strained SOI MOSFETs**
M. Seo[1,2], H. Bae[1], C.-H. Jeon[2], B.-H. Lee[2] and Y.-K. Choi[1]; *[1]School of Electrical Engineering, Korea Advanced Institute of Science and Technology Daejeon, Republic of Korea, [2]Semiconductor Business Samsung Electronics, Yogin-Si, Gyeonggi-Do, Republic of Korea*

6.4 **Self-Heating Assessment and Cold Current Extraction in FDSOI MOSFETs**
K. Triantopoulos[1,2], M. Cassé[1], L. Brunet[1], P. Batude[1], C. Fenouillet-Béranger[1], G. Reimbold[1], G. Ghibaudo[2]; *[1]CEA, LETI, MINATEC Campus, Grenoble, France, [2]IMEP-LAHC, Grenoble, France*

6.5 **Z²-FET SPICE Model: DC and Memory Operation**
S. Martinie[1], J. Lacord[1], O. Rozeau[1], M.-S. Parihar[2], K. Lee[2], M. Bawedin[2], S. Cristoloveanu[2], Y. Taur[3] and J-C. Barbe[1]; *1CEA-LETI, Grenoble, France. [2]University Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, Grenoble, France. [3]University of California, San Diego, USA*

6.6 **An Improved Mobility Model for FDSOI TriGate and Other Multi-Gate Nanowire MOSFETs Down to nm-Scaled Dimensions**
M. Cassé[1], J. Pelloux-Prayer[1], Z. Zeng[2], Y.-M Niquet[2], F. Triozon[1], S. Barraud[1], G. Reimbold[1]; *[1]CEA, LETI, MINATEC Campus, Grenoble, France, [2]INAC-MEM, LSIM, Grenoble, France*

SESSION 7: 3D WAFER STACKING

7.1 **TBA**
Sergey Shumarayev; *Intel, CA, USA (Invited Speaker)*

7.2 **Heterogeneous Integration toward Monolithic 3D Chip**
SH Kim[1], S-K. Kim[1], J-P. Shim[1], D-m. Geum[1], G. Ju[1], H. S. Kim[1], H. J. Lim[1], H. R. Lim[1], J-H. Han[1], CM. Kang[2], D. S. Lee[2], J. D. Song[1], W. J. Choi[1], H-j. Kim[1]; *[1]Korea Institute of Science and Technology (KIST), Korea, [2]Gwangju Institute of Science and Technology (GIST), Korea (Invited Speaker)*

7.3 **Integration of Si-CMOS and III-V Materials through Multi-wafer Stacking**
K. H. Lee[1], L. Zhang[1], B. Wang[1], S. C. Goh[1], S. Bao[1,2], Y. Wang[1], W. A. Sasangka[1], K. E. K. Lee[1], E. Fitzgerald[1,3], and C. S. Tan[1,2]; *[1]Singapore-MIT Alliance for Research and Technology (SMART), Singapore, [2]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, [3]Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA*

7.4 **A Novel in-Situ Resistance Measurement to Extract IMC Resistivity and Kinetic Parameter for CoSn 3D Stacks**
L. Hou[1,2], J. Derakhshandeh[1], J. De Coster[1], T. Wang[1], V. Cherman[1], P. Bex[1], K. J. Rebibis[1], G. Van De Plas[1], G. Beyer[1], E. Beyne[1], I. De Wolf[1,2]; *[1]IMEC, Leuven, Belgium, [2]Dept. Material Engineering, KU Leuven, Leuven, Belgium*

6:00PM SESSION 8: POSTER SESSION AND RECEPTION

8.1 **Low Temperature Influence on Long Channel STI Last Process Relaxed and Strained Ge pFinFETs**
A.V. Oliveira[1,2], P.G.D. Agopian[1,3], J.A. Martino[1], E. Simoen[2], J. Mitard[2], L. Witters[2], N. Collaert[2] and C. Claeys[2,4]; *[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, [2]Imec, Leuven, Belgium, [3]UNESP, Campus de São João da Boa Vista, Brazil, [4]E.E. Dept., KU Leuven, Belgium*

8.2 **Impact of the Zn Diffusion Process at the Source Side of InXGa1-XAs nTFETs on the Analog Parameters Down to 10 K**
C. Bordallo[1], J. Martino[1], P. Agopian[1,2], A. Alian[3], Y. Mols[3], R. Rooyackers[3], A. Vandooren[3], A. Verhulst[3], E. Simoen[3], C. Claeys[3,4], N. Collaert[3]; *[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, [2]UNESP, Univ. Estadual Paulista, São João da Boa Vista, Brazil, [3]Imec, Leuven, Belgium, [4]E.E. Dept, KU Leuven, Leuven, Belgium*

8.3 **Ultra Low Power Inductorless Low Noise Amplifier: Comparison of FDSOI Technologies**
J. Zaini[1,2], F. Hameau[1], B. Martineau[1], T. Taris[2], D. Morche[1] and P. Audebert[1]; *[1]CEA, LETI, MINATEC Campus, Grenoble, France, [2]IMS Laboratory, University of Bordeaux, Talence, France*

8.4 **Is there a Zero Temperature Bias Point (ZTC) on Back Enhanced (BE) SOI MOSFET?**
L. S. Yojo[1], R. C. Rangel[1,2], K. R. A. Sasaki[1], J. A. Martino[1]; *[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, [2]FATEC-SP, Faculdade de Tecnologia de São Paulo, São Paulo, Brazil*

8.5 New Method for Observing Self-Heating Effect Using Transistor Efficiency Signature
C. A. B. Mori[1], P. G. D. Agopian[1,2], J. A. Martino[1]; *[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, [2]São Paulo State University (UNESP), São João da Boa Vista, Brazil*

8.6 Lateral Spacers Influence on the Effective Channel Length of Junctionless Nanowire Transistors
R. Trevisoli, R. T. Doria, M. de Souza, M. A. Pavanello; *Centro Universitário FEI São Bernardo do Campo, Brazil*

8.7 Definite Influence of Substrate-Contact Condition on SOI Substrate Impedance Parameters
I. Yarita, S. Shingo and Y. Omura; *Kansai University, Suita, Osaka, Japan*

8.8 Study of Process Transconductance for Understanding Gate Capacitance of FDSOI NCFET
S. Qureshi and S. Mehrotra; *Department of Electrical Engineering, Indian Institute of Technology Kanpur, India*

8.9 Improving Solder Wetting of Micro Bumps on Metal Pads Using Metallic or Organic Pad Coatings
I. De Preter, L. Hou, J. Derakhshandeh, P. Bex, F. Fodor, V. Cherman, K. J. Rebibis, A. Miller, G. Beyer, E. Beyne; *IMEC, Leuven, Belgium*

8.10 PVT Compensation in Mie Fujitsu 55 nm DDC: A Standard-Cell Library Based Comparison
T. C. Müller[1,2], J-L. Nagel[1], M. Pons[1], D. Séverac[1], K. Hashiba[3], S. Sawada[3], K. Miyatake[3], S. Emery[1], A. Burg[2]; *[1]CSEM, Neuchâtel, Neuchâtel, Switzerland, [2]École polytechnique fédérale de Lausanne, Lausanne, Vaud, Switzerland, [3]Mie Fujitsu Semiconductor Ltd., Yokohama, Kanagawa, Japan*

8.11 Theoretical Models for Low-Frequency Noise Behaviors of Buried-Channel MOSFETs
Y. Omura and S. Sato; *Dept. of Electric, Electronics and Information Eng., Kansai University and ORDIST of Kansai University, Yamate-cho, Suita, Osaka, Japan*

8.12 14nm FinFET Technology SRAM Cell Margin Evaluation and Analysis by Local Layout Effect
S. Y. Mun[1], D. Burnett[2], KY Lim[1], S. Parihar[2], Y. Shi[1], H-C. Lo[1], W. Hong[1], K. Lee[1], O. Hu[1], J. Versaggi[1], C. Jerome[1], L. Lee[1], S. Samavedam[1], DK Sohn[1]; *[1]ATD 14NM Device, GLOBALFOUNDRIES, Malta, NY, USA, [2]Global Memory Solutions, GLOBALFOUNDRIES, Austin, TX, USA*

8.13 Design Optimization for NEM Relays Implemented in BEOL Layers
U. Sikder, T-J. King Liu; *Intel Department of EECS University of California, Berkeley, CA, USA*

8.14 Energy-Delay Tradeoffs of Low-Voltage Dual Mode Logic in 28nm FD-SOI
R. Taco[1], I. Levi[1], M. Lanuzza[2], A. Fish[1]; *[1]Bar-Ilan University, Ramat-Gan, Israel, [2]Univeristy of Calabria, Rende, Italy*

8.15 **A 2.9nW Ultra-Low Power Ripple-Voltage MPPT for Autonomous Miniature Sensor Nodes**
K. Lundager, and F. Moradi; *Department of Electrical and Computer Engineering, Aarhus University, Aarhus, Denmark*

8.16 **Hump-Effect Impact on Subthreshold VLSI Circuit**
M.Coustans[1], F. Krummenacher[1], M. Kayal[1], D. Gauthey[2], S. Rota[2], A. Acovic[3], P. Habas[3], R. Meyer[3]; *[1]Swiss Federal Institute of Technology (EPFL) Lausanne, Switzerland, [2]The Swatch Group Research and Development Ltd, Marin-Epagnier, Switzerland, [3]EM Microelectronic-Marin SA, Marin-Epagnier, Switzerland*

8.17 **Differential Input Output CMOS (DINO-CMOS) – High performance and Energy Efficient Logic Family**
M. Haber[1], I. Levi[1], Y. Joshua[2] and A. Fish[2]: [1]Student Member IEEE, [2]Member IEEE

8.18 **Secured Dual-Rail-Precharge Mux-Based (DPMUX) Symmetric-Logic for Low Voltage Applications**
D. Z. Zabib, I. Levi, A. Fish, O. Keren; *Faculty of Engineering, Bar-Ilan University, Israel*

8.19 **STI Techniques for Isolation of RF-SOI Devices**
S. Adusumilli, S. Shank, J. Ellis-Monaghan, C-h. Teng, M. Levy, A. Stamper; *RF Technology Development, Fab 9, GLOBALFOUNDRIES, Essex Junction Vt, USA*

8:00PM **RUMP SESSION**

TUESDAY OCTOBER 17, 2017

7:00AM CONTINENTAL BREAKFAST

8:00AM SESSION 9: RF CIRCUITS

9.1 **Opportunity of CMOS FD-SOI for RF Power Amplifier**
B. Martineau, E. Mercier and P. Vincent; *CEA-LETI, Grenoble, France Université de Grenoble-Alpes, Grenoble, France*

9.2 **A High-Efficiency Single-Stage Power Amplifier for WLAN 802.11ac in 22nm FDSOI**
S. T. Lee, A. Bellaouar and S. Embabi; *Globalfoundries, Richardson, TX, USA*

9.3 **A Study of Interferences inside An RF Switch Array in 45nm SOI CMOS**
C. Wang[1], F. Lu[1], Q. Chen[1], F. Zhang[1], C. Li[1], D. Wang[2], and A. Wang[1]; *[1]Dept. of ECE, University of California, Riverside, CA, USA; [2]Global Foundries, USA*

9.4 **Improving Noise and Linearity of CMOS Wideband Inductorless Balun LNAs for 10-GHz Software-Defined Radios in 28nm FDSOI**
C. Gimeno, F. Stas, G. de Streel, D. Bol, and D. Flandre; *ICTEAM Institute, Université Catholique de Louvain, Louvain-la-Neuve, Belgium*

9.5 **A Wide Range 60 GHz VCO Using Back-Gate Controlled Varactor in 22 nm FDSOI Technology**
C. Zhang[1] and M. Otto[2]; *[1]GLOBALFOUNDRIES, Austin, TX, USA, [2]GLOBALFOUNDRIES, Dresden, Germany*

SESSION 10: EMBEDDED MEMORIES

10.1 **HfO2 Based Ferroelectric Memories: From Physical Modeling to Circuit Models of Ferroelectric Memory Devices**
Milan Pesic; *NaMLab gGmbH, Dresden, Germany (Invited Speaker)*

10.2 **Review of Progress in Understanding the Electron Transport Properties of Amorphous Chalcogenide Phase Change Semiconductors**
J. Liu; *Department of Electrical Engineering, University of Washington, Seattle, WA, USA (Invited Speaker)*

10.3 **TBA**
Luc Thomas; *Headway Technologies Inc., Milpitas, CA, USA (Invited Speaker)*

10.4 **32Kb Innovative Fuse (I-Fuse) Array in 22nm FD-SOI with 0.9V/1.4mA Program Voltage/Current and 0.744um2 Cell**
S. Chung, W-K. Fang, J. Lin, W-H. Yu, and JY Hsiao; *Attopsemi Technology Co., LTD, Hsinchu, Taiwan*

10:00AM BREAK

10:20AM **SESSION 11: SOI WAFERS**

11.1 **Novel CV/GV Technique for Top and Bottom BOX Interfaces Traps Density Extraction on FDSOI Wafers**
W. Vandendaele[1], C. Malaquin[2], A. Ghorbel2, M. Cassé[1], F. Allibert[2], G. Reimbold[1]; *[1]CEA LETI - MINATEC Campus, Grenoble, France, [2]SOITEC SA, Parc Technologique des Fontaines, Bernin, France*

11.2 **A SPDT RF Switch Small- and Large-Signal Characteristics on TR-HR SOI Substrates**
B. Kazemi Esfeh[1], S. Makovejev[2], F. Allibert[3] and J.-P. Raskin[1]; *[1]ICTEAM, Université catholique de Louvain, Louvain-la-Neuve, Belgium, [2]Incize, Louvain-la-Neuve, Belgium, [3]Soitec, Bernin, France*

11.3 **Time-Dependent Vth Shift of Silicon on Thin BOX under Large Back Bias**
Y. Yamamoto, H. Makiyama, T. Hasegawa, S. Okanishi, K. Maekawa, H. Shinkawata and Y. Yamaguchi; *Renesas Electronics Corporation Device Technology Division, Advanced Device Technology Department, Hitachinaka-shi Ibaraki, Japan*

11.4 **Enhanced Silicon-On-Insulator Platform Enabling New Structures and Applications**
A. Haapalinna[1], T. Aalto[2]; *[1]Okmetic Oy, Vantaa, Finland, [2]VTT, Espoo, Finland*

SESSION 12: LOW POWER CIRCUITS 1

12.1 **FDSOI Body-Biasing Techniques for Circuit Design Optimization**
Ravi Vaidyanathan, Paul Grudowski; NXP Semiconductors (Invited Speaker)

12.2 **A 28 nW CMOS Supply Voltage Monitor for Adaptive Ultra-Low Power IoT Chips**
D. A. Kamakshi, H. N. Patel, A. Roy, and B. H. Calhoun; *Dept. of Electrical Engineering, University of Virginia, Charlottesville, Virginia, USA*

12.3 **Design Margin Elimination Through Robust Timing Error Detection at Ultra-Low Voltage**
H. Reyserhove and W. Dehaene; *KU Leuven, ESAT-MICAS, Kasteelpark Arenberg, Leuven, Belgium*

12.4 **A Subthreshold 30pJ/bit Self-timed Ring Based True Random Number Generator for Internet of Everything**
M. Coustans[1], C. Terrier[2], T. Eberhardt[2], S. Salgado[2], A. Cherkaoui[3], L. Fesquet[3]; *[1]Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, [2]EM Microelectronic-Marin SA, Marin-Epagnier, Switzerland, [3]Univ. Grenoble Alpes & CNRS, TIMA, Grenoble, France*

12.5 **0.45v and 18µA/MHz MCU SOC with Advanced Adaptive Dynamic Voltage Control (ADVC)**
U. Zangi[1], N. Feldman[1], J. Shor[2], A. Fish[2]; *[1]PLSense, Yokneam Israe, [2]Bar Ilan University, Ramat Gan, Israel*

12:20PM **LUNCH** *(ON OWN)*

1:20PM **SESSION 13: ADVANCED SOI DEVICES 2**

13.1 **3D Technologies for Analog/RF Applications**
Anne Vandorren; imec, Leuven, Belgium (Invited Speaker)

13.2 **Advanced FDSOI Design: The U-channel Device for 7nm Node and Beyond**
R. Muralidhar, R. Dennard, T. Ando, I. Lauer, and T. Hook; *IBM T J Watson Research Center, Yorktown heights, NY (Invited Speaker)*

13.3 **Gate-induced vs. implanted body doping impact on Z²-FET DC operation**
C. Navarro[1], F. Gamiz[1], N. Rodriguez[1], L. Donetti[1], C. Sampedro[1], S. I. Kim[2], Y. T. Kim[2], S. Cristoloveanu[3]; *[1]University of Granada, Granada, Spain, [2]Korean Institute of Technology, Seoul, Republic of Korea, [3]IMEP-LAHC, Grenoble, France*

13.4 **Experimental Comparative Analysis between Junctionless and Inversion Mode Nanowire Transistors down to 10 nm-Long Channel Lengths**
R. T. Doria[1], R. Trevisoli[1], M. de Souza[1], M. A. Pavanello[1], M. Vinet[2], M. Cassé[2], O. Faynot[2]; *[1]Centro Universitário FEI, São Bernardo do Campo, Brazil, [2]CEA, LETI, Minatec Campus, Grenoble, France*

SESSION 14: LOW POWER CIRCUITS 2

14.1 **On the Road Towards Commercializing Ultra-Low-Vdd SoC for Internet-of-Things**
Yu Pu; Qualcomm Research (Invited Speaker)

14.2 **Optimizing TSPC Frequency Dividers for Always-On Low-Frequency Applications in 28nm FDSOI CMOS**
P. Xu and D. Bol; *ECS group, ICTEAM institute, Université catholique de Louvain, Belgium*

14.3 **An Ultra-Low-Power Dual-Phase Latch Based Digital Accelerator for Continuous Monitoring of Wheezing Episodes**
P. Gonzalez-Guerrero and M. Stan; *University of Virginia*

14.4 **An Ultra-Low-Power FPGA for IoT Applications**
H. Qi, O. Ayorinde, and B. H. Calhoun; *Dept. of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA*

3:20PM **BREAK**

3:40PM **SESSION 15: ADVANCED SOI TECHNOLOGY**

15.1 **How to Leverage SOI Platforms to Achieve Optimum Power Efficiency?**
Manuel Sellier; *Soitec (Invited Speaker)*

15.2 **TBA**
Franck Arnaud; *STMicroelectronics, Crolles, France (Invited Speaker)*

SESSION 16: LOW VOLTAGE DEVICES 1

16.1 **New Steep-Slope Device of Comprehensive Properties Enhancement with Hybrid Operation Mechanism for Ultra-Low-Power Applications**
R. Huang, Q. Huang, Y. Zhao, C. Chen, R. Jia, C. Wu, J. Wang, L. Guo and Y. Wang; *Peking University, Peking, China (Invited Speaker)*

16.2 **Experimental Analysis of Differential Pairs Designed with Line Tunnel FET Devices**
M. D. V. Martino[1], J. A. Martino[1], P. G. D. Agopian[1,2], R. Rooyackers[3], E. Simoen[3], N. Collaert[3], and C. Claeys[3,4]; *[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil, [2]São Paulo State University (UNESP), Campus São João da Boa Vista, Brazil, [3]Imec, Leuven, Belgium, 4E.E. Dept, KU Leuven, Leuven, Belgium*

16.3 **A 11.5pW/bit 400mV 5T Gain-Cell eDRAM for ULP Applications in 28nm FD-SOI**
R. Giterman, A. Teman, and A. Fish; *Faculty of Engineering, Bar-Ilan University, Ramat Gan, Israel*

16.4 **Investigation of Short-Channel Effects in 2D Negative-Capacitance Field-Effect Transistors**
W-X. You, C-P. Tsai, and P. Su; *Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan*

6:00PM **E3S POSTER SESSION AND RECEPTION**

8:00PM **COOK OUT**

WEDNESDAY OCTOBER 18, 2017

7:00AM CONTINENTAL BREAKFAST

8:00AM SESSION 17: NEUROMORPHIC COMPUTING 1

17.1 The N3XT Technology for Brain-Inspired Computing
Philip Wong; *Stanford University, Stanford CA, USA (Invited Speaker)*

17.2 System-Level Benchmark of Synaptic Device Characteristics for Neuro-Inspired Computing
P-Y. Chen, X. Peng, and S. Yu; *School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ*

17.3 Machine Intelligence through 3D Waferscale Integration
Arvind Kumar, *IBM T.J. Watson Research Center, Yorktown Heights, NY, USA (Invited Speaker)*

SESSION 18: MONOLITHIC 3D 2

18.1 Monolithic Integration of Multiple III-V Semiconductors on Si for Nanoelectronics
Heinz Schmid; IBM Research, Zürich, Switzerland (Invited Speaker)

18.2 GOI fabrication for Monolithic 3D integration
A. Abedin, L. Zurauskaite, A. Asadollahi, K. Garidis, G. Jayakumar, B.G. Malm, P.-E. Hellström* and M. Östling; *Department of Electronics KTH Royal Institute of Technology Stockholm, Sweden*

18.3 A 1,000x Improvement in Computer Systems by Bridging the Processor-Memory Gap
Z. Or-Bach; *MonolithIC 3D Inc., San Jose, CA*

10:00AM BREAK

10:20AM SESSION 19: NEUROMORPHIC COMPUTING 2

19.1 Analog Circuits for Mixed-Signal Neuromorphic Computing Architectures in 28 nm FD-SOI Technology
N. Qiao and G. Indiveri; *Institute of Neuroinformatics University of Zurich and ETH Zurich Zurich, Switzerland (Invited Speaker)*

19.2 TBA
Zhengya Zhang; *University of Michigan, Ann Arbor, MI, USA (Invited Speaker)*

19.3 **Three-Dimensional Wafer Scale Integration for Ultra large Scale Cognitive Systems**
Zhe Wan and S.S. Iyer; *UCLA, Los Angeles, CA, USA (Invited Speaker)*

19.4 **TrueNorth: from Hardware to Ecosystem**
John Arthur; *IBM Research (Invited Speaker)*

SESSION 20: HETEROGENEOUS INTEGRATION

20.1 TBA
Dimitri Strukov; *University of Santa Barbara, Santa Barbara, CA, USA (Invited Speaker)*

20.2 **New Thermal Management Approach for Transistor-level 3-D Integtration**
M. A. Iqbal, M. Rahman; *Computer Science Electrical Engineering, University of Missouri-Kansas City, Kansas City, MO, USA*

20.3 **Hybrid Silicon CMOS-Carbon Nanotube Cryptographic Key Generator**
D. Armstrong, B. Nasri, R. Karri, and D. Shahrjerdi; *Electrical and Computer Engineering, New York University, Brooklyn, New York*

20.4 **Die-Level Processing for 3-D Monolithic Integration of Piezoelectric MEMS on CMOS**
A. R. Colon-Berrios, H. Edrees, D. De Godoy, P. Kinget and I. Kymissis; *Electrical Engineering Department, Columbia University, New York, NY, USA*

12:20PM **LUNCH** *(ON OWN)*

1:20PM **SESSION 21: FDSOI CIRCUITS 2**

21.1 **System Level FDSOI Exploration and Integration**
Jeff Cunningham*; NXP Semiconductors (Invited Speaker)*

21.2 **A 65-nm SOTB Implementation of a Physically Unclonable Function and Its Performance Improvement by Body Bias Control**
Y. Hori, T. Katashita, and Y. Ogasahara; *National Institute of Advanced Industrial Science and Technology (AIST) Tsukuba Central 2, Tsukuba, Ibaraki, Japan*

21.3 **Physical Implementation of Low Power SoC Chip in SEC 28nm FD-SOI**
J. Zhu; VeriSilicon, Shanghai, China

21.4 **A 0.148nJ/conversion 65nm SOTB Temperature Sensor LSI Using Thermistor-defined current source**
S. Nii and K. Ishibashi; *The University of Electro-Communications Tokyo, Japan*

SESSION 22: PRECISSION WAFER BONDING

22.1 **1µm Pitch Direct Hybrid Bonding with <300nm Wafer-to-Wafer Overlay Accuracy**
A. Jouve[1], V. Balan[1], N. Bresson[1], C. Euvrard-Colnat[1], F. Fournel[1], Y. Exbrayat[1], G. Mauguen[1], M. Abdel Sater[1], C. Beitia[1], L. Arnaud[1], S. Cheramy[1], S. Lhostis[2], A. Farcy[2], S. Guillaumet[2], S. Mermoz[2]; *[1]CEA, LETI, University Grenoble Alpes, Grenoble, France MINATEC Campus, Grenoble, France, [2]STMicroelectronics, Crolles, France*

22.2 **Mass Production Equipment Technology for 300mm Wafer-Level Fusion Bonding**
T. Kawauchi; *3D-Integration Division, Tokyo Electron Limited (Invited Speaker)*

3:20PM BREAK

3:40PM SESSION 23: LOW VOLTAGE DEVICES 2

23.1 **Investigation of Backgate-Biasing Effects on Ultra-Thin-Body GeSn Based Tunneling FET**
H. Wang[1], G. Han[1], Y. Liu[1], J. Zhang[1], Y. Hao[1], X. Jiang[2]; *[1]State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an, Shaanxi, China, [2]State Key Laboratory of Supperlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing China*

23.2 **Balancing Pull-In and Adhesion Stability Margins in Non-Volatile NEM switches**
G. Usai[1], L. Hutin[1], U. Sikder[2], J. L. Muñoz-Gamarra[1], T. Ernst[1], T. J. King Liu[2], M. Vinet[1]; *[1]CEA Leti Minatec Campus, Grenoble, [2]University of California at Berkeley, EECS Department, Berkeley, CA*

23.3 **Projected Performance of Experimental InAs/GaAsSb/GaSb TFET as Millimeter-Wave Detector**
J. Zhang[1], C. Alessandri[1], P. Fay[1], A. Seabaugh[1], T. Ytterdal[2], E. Memisevic[3] and L. E. Wernersson[3]; *[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA, [2]Department of Electronic Systems Norwegian University of Science and Technology Trondheim, Norway*

23.4 **High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology**
Y-T. Wu[1], M-H. Chiang[1], J. F. Chen[1], F. Ding[2], D. Connelly[2], and T-J. King Liu[2]; *[1]Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Taiwan, R.O.C, [2]Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA, USA*

23.5 Analog Performance of Self-Cascode SOI Nanowires nMOSFETs Aiming at Low-Power Applications

R. Assalti[1], M. de Souza[1], M. Cassé[2], S. Barraud[2], G. Reimbold[2], M. Vinet[2] and O. Faynot[2]; *[1]Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil, [2]Département des Composants Silicium – SCME/LCTE, CEA-LETI Minatec, Grenoble, France*

SESSION 24: MONOLITHIC 3D 3

24.1 Layered Semiconductors for Monolithic 3D Integration

Angada Sachid; *UC Berkeley, Berkeley, CA, USA (Invited Speaker)*

24.2 Reliability Analysis on Low Temperature Gate Stack Process Steps for 3D Sequential Integration

A.Tsiara[1,2], X.Garros[1], C.-M.V.Lu[1], C.Fenouillet-Béranger[1], P.Batude[1], R.Gassilloud[1], F.Martin[1], O.Faynot[1], G.Ghibaudo[2] and G.Reimbold[1]; *[1]CEA, LETI, MINATEC Campus, [2]IMEP-LAHC*

24.3 Towards 500°C SPER activated devices for 3D Sequential Integration

J. Micout[1,2], B. Sklenard[1], P. Batude[1], R. Berthelon[1,3], Q. Rafhay[2], J. Lacord[1], B. Mathieu[1], L. Pasini[1,2,3], Z. Saghi[1], V. Delaye[1], L. Brunet[1], C. Fenouillet-Beranger[1], S. Joblot[3], F. Mazen[1], V. Mazzocchi[1], J-P. Colinge[1], G. Ghibaudo[2] and M. Vinet[1]; *[1]CEA, Leti, MINATEC Campus, Univ. Grenoble Alpes, [2]IMEP-LAHC, MINATEC/INPG, Univ. Grenoble Alpes, [3]STMicroelectronics*

24.4 A Partitioning-Free Methodology for Optimized Gate-Level Monolithic 3D Designs

O. Billoint[1], M. Brocard[1], S. Thuries[1], G. Berhault[1], H. Sarhan[2]; *[1]Univ. Grenoble Alpes, Grenoble, France, [2]MENTOR GRAPHICS, Montbonnot-Saint-Martin, France*

24.5 Generalized Cost Model for 3D Systems

D. Gitlin[1], M. Vinet[2], S. Cheramy[2], H. Metras[2], O. Faynot[2], T. Signamarcheix[2] and J-R. Lequepeys[2]; *[1]Scientific Advisor & Independent Consultant to CEA-Leti Palo Alto, CA, [2]CEA Leti, MINATEC Campus, Grenoble, France*

AWARDS AND CLOSING REMARKS

3D TUTORIAL
TUESDAY 2:20PM

THIS TUTORIAL IS INCLUDED IN THE CONFERENCE TECHNICAL PROGRAM REGISTRATION

Three dimensional chips stacked using Through Silicon Via (TSV) technology has been under consideration and the subject of intensive research for several years now.

This tutorial covers the technology, applications, design and CAD for 3DIC. The technology will be introduced, including TSVs, face to face technologies, integration options and interposers. Applications will be discussed as driven by cost, performance and power efficiency needs.

Examples will be given from the commercial world and the author's own research. CAD and CAD-driven design will be covered including verification, test, and thermal evaluation.

Topics that will be covered are:

Design for 2.5D- and 3D-Stacked ICs
PAUL FRANZON, *NORTH CAROLINA STATE UNIVERSITY*

1. 3DIC Motivation
2. 3DIC Manufacturing
3. 3DIC Design
4. Test
5. Conclusions and Future Perspectives

Overview of Monolithic 3D IC Processing
ZVI OR-BACH, *MONOLITHIC 3D™ INC.*

1. Forming the Silicon Layer: Crystallization, layer transfer
2. Forming Transistors: Modify process, split hot/cold, shield the underlying structure
3. Transfer Yet Align: Smart process, precise bonder, smart alignment
4. Non CMOS Transistors: CNT, mechanical and triode base transistors.
5. New Breakthroughs: Monolithic 3D using current fab process
6. Killer Application: Solving the memory wall

FDSOI SHORT COURSE

THURSDAY FULL DAY COURSE

THE FDSOI SHORT COURSE IS AVAILABLE FOR AN ADDITIONAL FEE AND INCLUDES A LIGHT BREAKFAST AND LUNCH. PRESENTATION MATERIALS WILL BE PROVIDED ON A USB DRIVE.

On Thursday, the IEEE S3S Conference will host a full-day FDSOI Short Course, which brings in experts from the academia and industry to teach different aspects of circuit design in FDSOI.

Given the FDSOI technology offering at multiple foundries and multiple nodes, including 65nm, 28nm and 22nm, we believe this is a unique and timely opportunity for circuit designers to learn first-hand from distinguished experts and bring in their questions and concerns.

In addition to the following lectures, EDA vendors, IP vendors and foundry technologists will be available for in-depth discussions during break-outs and poster session.

8:00AM **Welcome**

8:30AM **Fundamentals of FDSOI Design**
Yoshiki Yamamoto*; Renesas*

Body Biasing Techniques and Body Bias Generators
Andreas Burg*; EPFLF*

10:00AM **COFFEE BREAK -** Discussion with EDA & IP Vendors

10:30AM **FDSOI Platforms and Applications**
Jeff Cunningham*; NXP Semiconductors*

TBA
Jiong Zhu*; Verisilicon*

12:00PM **LUNCH** *(Provided with course)*

Ultra-Low Voltage and Ultra-Low Power Designs for IoT
Sebastien Thuries*; CEA Leti*

High Speed Analog Design
Yusuf Leblebici*; EPFL*

3:00PM **COFFEE BREAK -** Discussion with EDA & IP Vendors Poster Session

4:15AM **Analog and RF Design in FDSOI**
Carlo Tinella*; Asygn*

RF Design in FDSOI
Baudouin Martineau*; Leti*

RUMP SESSION
MONDAY 8:00PM

SEMICONDUCTOR TECHNOLOGIES DRIVING ARCHITECTURES FOR BRAIN-LIKE EFFICIENT AI

ALI KESHAVARZI; *Leading Edge Research, LLC (Moderator)*

AI is enabling a variety of applications such as voice and image recognition cost-effectively with low power. As such it is receiving a wide range of attention in public. AI is highly debated among technical communities while commercial companies are rushing for business opportunities. Semiconductor materials, devices, integration techniques and technologies are being probed to enable architectures for AI systems and applications.

Silicon-based semiconductor technology has driven efficient compute per watt for example in the case of application processors utilizing advanced technology nodes with established von Neumann architecture in pervasive mobile devices. Energy-efficient computing measured in MIPS/W is paramount for AI and for the future. The key question is: What drives MIPS/W to achieve efficiency in the range of human brain? What semiconductor technologies will guide architectures behind brain-like energy-efficient computing that is required for AI?

A panel of experts will be discussing and debating various technical directions and market opportunities while exploring various approaches. Technical topics span the range of materials/processes/devices/circuits/integration schemes that are driving architectures toward establishing power efficient AI.

SATELLITE FUNCTIONS

E3S POSTER SESSION AND RECEPTION
Tuesday 6:00 PM

5th Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistor Workshop

The 2017 Berkeley Symposium on Energy Efficient Electronic Systems will take place October 19-20 at the campus of the University of California, Berkeley. Established in 2009 the goal of this event is to bring together researchers in academia, industry, and national labs from around the world working on breakthroughs in next generation low-energy information processing systems. This year, the Berkeley Symposium will join forces with the Steep Transistors Workshop in a two-day event to further expand its reach and impact. The joint event will focus on the challenges and opportunities in low-energy information processing systems, extending from new low-power nanoelectronic devices, through circuit design, chip-scale architecture, short-range interconnects, long-range interconnect, networks, software, storage systems, servers data centers and supercomputers.

On Tuesday, October 17, we host a poster session and reception covering some of the work that will be presented at E3S to give a glimpse of this symposium to S3S attendees.

COOLCUBE™/3DVLSI OPEN WORKSHOP
Tuesday

This year, Leti and Qualcomm are organizing a CoolCube™/3DVLSI open Workshop dedicated to High Density 3D-IC Technologies including Monolithic 3D Integration (called CoolCube™ Technology at Leti).

The extended CoolCube™ project's goals include building a complete ecosystem that takes the technology from design to fabrication. A first CoolCube™/3DVLSI open Workshop was organized by Leti and Qualcomm in San Diego back in 2014. Now, the Workshop has become a forum for industrial partners and ecosystem to share research and development progress in making innovative High Density 3D technologies a truly feasible path towards 3DVLSI industrialization for reliable and cost effective products.

An agenda will be sent early September. A first session will be dedicated to update on Technologies and Design Enablement by both Leti and Qualcomm. Then during a second session, all partners and attendees are invited to share ideas, solutions, studies and progress related to the emerging 3D-IC technologies.

Registration is free and available to S3S attendees.
Since seating is limited, registration is by invitation only.
If interested, please send an email to jean-eric.michallet@cea.fr

OTHER FUNCTIONS

COOKOUT
Tuesday 8:00PM

Our conference would not be complete without our cookout. Combining great food and pleasant company is all part of what makes our conference so special. The cookout is another great way to network and meet your fellow attendees. Relax and enjoy yourself.

HOSPITALITY SUITE
Monday thru Wednesday 10:00AM to 6:00PM

This year we will have for our member's convenience a hospitality suite located in the hotel. This will be a location that everyone will have access to during conference hours. Think of it as a place where you can get away from conference proper. Sit down in comfortable surroundings and enjoy a conversation with colleagues. Have a light refreshment and just get away from things for a few minutes.

BREAKFAST
Monday thru Wednesday 7:00AM to 8:00AM

Remember to start your day right!

One of the perks of the Technical or Combined Membership is a light breakfast daily (Monday thru Wednesday). Don't worry, our breakfast also includes coffee for those who need more that a bite of food to get them started.

Networking Reception
Wednesday Following Conference Close

Saying good-bye is never easy.

So why not extend your stay a little while and join us for an evening of networking.

Whether you are joining us Friday for the FDSOI Short Course or just hanging out waiting for your pl. Our Wednesday evening reception is a great way to close out the technical portion of the conference.

HYATT REGENCY SAN FRANCISCO AIRPORT

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Located in Burlingame, California, the Hyatt Regency San Francisco Airport hotel allows visitors to access the Bay Area with ease. The Hyatt Regency SFO provides a convenient location for any traveler with close proximity to San Francisco International Airport and the city.

The Hyatt Regency San Francisco Airport just completed a full renovation of their guestrooms rooms. Just minutes from San Francisco International Airport (SFO), our Burlingame hotel offers free Wi-Fi, in the sleeping rooms. A complimentary 24-hour airport shuttle service is available for your convenience.

Looking for a bite to eat? The 3SIXTY Restaurant offers fresh, health-conscious food items for those with no time to wait and a comfortable and entertaining surrounding for diners looking for a more traditional restaurant environment. Open from 6:30am to 10:00pm daily. There are also restaurants within a reasonable walking distance of the facility as well as well as others within a short drive.

Hotel Rates

The Hyatt Regency San Francisco Airport is pleased to offer a special discounted rate of $239.00 plus 12% occupancy tax single/double occupancy for conference attendees.

The rate will be good from Saturday, October 14th, 2017 thru Friday, October 19th, 2017 and are available three days prior and post if you wish to take a little extra time in the area. A major credit card or deposit will be needed when you make a reservation to guarantee your room

Our conference is in the heart of the tourist season in the bay area. As such, please make sure to reserve your room by September 16, 2016 to ensure availability. If you have a problem making a reservation, please contact the Conference Manager for assistance. manager@s3sconference.org

All hotel reservations must be made by **5:00pm PST, 20 September 2017**.

Student Rate Rooms

We have a few rooms available for students at a discounted rate. First priority will go to those students who are presenting papers. Please contact manager@S3Sconference.org for assistance.

Government Rate Rooms

Government rates are available at the prevailing rate. If you qualify for this rate, you will need to use this Government Rate Link to reserve your room. Please make sure when registering for your room, it is the same name you have registered with the conference.

Make a Reservation

Use the following link to reserve your room today! RESERVE YOUR ROOM NOW

Visit our website for additional hotel information

AIRPORT

The nearest international airports is San Francisco International Airport (SFO). This is largest airport and has the most options for both international and domestic travel. The Hyatt Regency San Francisco Airport offers free shuttle service from this airport only.

San Jose International Airport (SJC), is a smaller airport located 33 miles away. Standard travel time between this airport and the Hyatt Regency San Francis-co Airport is approximately 40 minutes via auto.

SHUTTLE SERVICE

The Hyatt San Francisco Airport offers a free 24-hour shuttle to and from San Francisco Airport. The shuttles run every 10 to 15 minutes from 5am to mid-night. It runs every 30 minutes between midnight and 5am. The shuttle can be picked up on the Upper level (not the baggage level) in the area clerarly marked for Hotel Shuttles.

If you are traveling in from San Jose International Airport (SJC), we suggest you use Super Shuttle or use the BART System to the Millbrae BART station. The Hyatt Regency San Francisco Airport is about two miles from teh Millbrae Bart Station

LOCAL TRANSPORTATION

The BART system is a great wat to get around. The Millbrae BART Station is a 35-minute walk or a 6-minute car drive. From the station you can access any-where the BART system reaches.

RENTAL CARS

The San Franciso International Airport (SFO) offers representation from all the major car rental companies. For a complete listing and contact information please see SFO Rental Cars.

The San Jose International Airport (SJC) offers a more limited selsction of car rental companie from which to choose. For a complete listing and contact information please see SJC Rental Cars.

PARKING AT THE HYATT

Hyatt Regency San Francisco Airport self-parking daily is $6 up to one hour, $12 up to six hours and $25 for over six hours.

Valet Parking daily is $10 up to one hour, $20 up to six hours and $30 for over six hours.

INTERNATIONAL TRAVELERS

For information on traveling to the United States. Please vistion the U.S. Department of State website for the most current information.

If you find you are in need of a Visa, contact manager@s3sconference.org for information on obtaining a letter for your embassy.

ON-SITE 2017 CONFERENCE REGISTRATION SCHEDULE

Sunday, October 15	6:00PM to 8:00PM
Monday, October 16	7:00AM to 5:00PM
Tuesday, October 17	7:00AM to 5:00PM
Wednesday, October 18	7:00AM to 12:00PM
Thursday, October 19	7:00PM to 12:00PM

CREDIT CARD PAYMENTS

To pay by credit card please use our ONLINE registration form.

We accept Visa, Master-Card and American Express. You will need to have the card with you when registering as you need to provide the security code when you enter your card information.

The 3-digit security code for Visa and MasterCard is located on the back of the card. The 4 digit code for American Express is located on the front of the card.

CHECK PAYMENTS

Complete the registration form and mail it with your check to:
IEEE S3S Conference, 6930 De Celis Place, #36, Van Nuys, CA 91406
Please make the check payable to 2016 IEEE S3S Conference.

All checks must be drawn on a US bank and in US funds only.

Registration forms received without payment will not be honored.

WIRE TRANSFER PAYMENTS

While payment may be made via bank transfer (by wiring funds), it is discouraged and there is an additional $25 fee per transfer to cover handling costs. If a bank transfer is necessary, please contact the conference manager at manager@s3sconference.org for further instructions and the appropriate account numbers.

CANCELLATIONS

Cancellation requests must be made in writing to the conference manager. Refund requests received by September 22, 2017 will receive a refund of registration fees less a $50 processing fee.

All refunds will be processed after the conference.

If you have any questions please do not hesitate to contact the conference manager at manager@s3sconference.org or call (818) 795-3768

REGISTRATION

SOI-3DI-Subthreshold Microelectronics Technology Unified Conference

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NAME TO APPEAR ON BADGE

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Do you have any special needs or dietary restrictions?
If YES - Please let us know so we can attempt to accommodate your needs:

*As you want it to appear on the Conference List of Attendees

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- Wire Transfers must be approved in advance and are subject to a $25 fee.
- No telephone registrations will be available

REGISTRATION FEES

Advance registration fees apply to completed forms and payment received by **September 25, 2017**

Combined Conference and Short Course

(Monday thru Thurs)	*by Sept 25th*	*After Sept 25th*	
IEEE Member	☐ $900	☐ $975	$ 0.00
Non Member	☐ $1125	☐ $1225	$ 0.00
Student IEEE Member	☐ $425	☐ $500	$ 0.00
Student Non Member	☐ $525	☐ $620	$ 0.00

Technical Program Only (Monday thru Wednesday)

IEEE Member	☐ $600	☐ $650	$ 0.00
Non Member	☐ $750	☐ $800	$ 0.00
Student IEEE Member	☐ $330	☐ $380	$ 0.00
Student Non Member	☐ $400	☐ $450	$ 0.00

Short Course Only (Thursday)

IEEE Member	☐ $400	☐ $450	$ 0.00
Non Member	☐ $450	☐ $500	$ 0.00
Student IEEE Member	☐ $125	☐ $150	$ 0.00
Student Non Member	☐ $175	☐ $200	$ 0.00

3D Tutorial Only (Tuesday 2:00pm)

IEEE Member	☐ $75	$ 0.00
Non Member	☐ $100	$ 0.00
Student IEEE Member	☐ $50	$ 0.00
Student Non Member	☐ $75	$ 0.00

Total Registration Fees $ 0.00

We welcome guests at our cookout.
The cookout is included with the purchase of the Technical Program, so you do not need to purchase again.
Below is for any guests you would wish to bring with you.

Wednesday Guest Cookout ☐ @ $80 ea. = $ 0.00

TOTAL ENCLOSED $ 0.00

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