2016

IEEE S3S Conference

10 – 13 October 2016, Hyatt Regency San Francisco Airport

2016 IEEE S3S Conference Call for Papers

IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (IEEE S3S)
"Energy Efficient Technology for the Internet of Things"

The 2016 IEEE S3S Conference will take place October 10th – 13th in San Francisco, CA. This industry-wide event gathers together widely known experts, contributed papers and invited talks focused on SOI Technology, Low-Voltage Devices/Circuits/Architectures, and 3D Integration.

A special focus area of the Conference in 2016 will be on energy efficient computation and communication to empower small systems. This is a timely topic given projections that the number of internet–connected devices will grow to 75 billion by 2020. Energy-efficiency is key to enabling small, battery-powered sensors and wireless connectivity hubs. The IEEE S3S organizers are pleased that the core technologies of the S3S Conference are sure to play critical roles in efficient computation and communication in energy starved systems.

In addition to over 100 contributed and invited papers, the conference will hold a Keynote and a Hot Topics session featuring distinguished speakers from industry and academia. The latter, focused on the Internet of Things, will address key topics such as IoT systems requirements, ultra-low power design and process, system integration or hardware security. It will illustrate the synergy between, and relevance of the SOI, Sub Vt and 3D axes of the conference as part of the roadmap for the coming years. We hope that these topics will provide inspiration for novel research, development, and collaboration throughout the S3S' core technology areas.

For the first time, the S3S Conference will be including two Tutorials free-of-charge with Conference registration. The first will cover FDSOI Circuit Design led by industry experts from the SOI Consortium. The second will introduce Technologies for monolithic 3D Integration. On Monday, we will also offer a full-day short course on Energy Efficient Computing and Communications including RF circuit technology. Panel Discussions, a Poster Session, and networking opportunities round out the program.

This year we have expanded the range of the "Subthreshold Microelectronics" area to "Low-Voltage Microelectronics", as with continued device scaling and lowering of threshold voltage the most energy efficient operating point is now often near-threshold and not below threshold.
The authors of selected papers will be invited to submit extended versions of their papers to a dedicated issue of the Journal of Low Power Electronics and Applications.

Finally, we are pleased to announce that the Conference will be offering a Best Paper Award and a Best Student Paper Award. The Best Student Paper Award includes a **$1,000 prize** from one of our industry sponsors.

Abstracts are solicited in all of the areas described in more detail below. We look forward to seeing you in San Francisco!

SUBMISSION INFORMATION

Prospective authors should prepare a 2-page abstract of their original work. Guidelines for abstracts can be found on our website at: **http://s3sconference.org.** Submissions will be accepted for review in PDF format only and should be e-mailed to: **papers@s3sconference.org**

Deadline for submissions is April 15, 2016

EXECUTIVE COMMITTEE

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Silicon On Insulator (SOI)

Ever increasing demand and advances in SOI and related technologies make it essential to meet and discuss new gains and accomplishments in the field. For over 35 years our conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-On-Insulators technology. Previously unpublished papers are solicited in all areas of SOI technology and related devices, circuits and applications, including:

- Device Physics and Modeling
- High-Voltage Devices
- Advanced Materials, Substrate & Process Integration
- Photonics
- New SOI Structures, Circuits and Applications
- Asynchronous Circuits
- Sensors, NEMS, and MEMS
- SOI and FDSOI Manufacturability and Process Integration
- Substrate Engineering
- Fully-Depleted / Thin-Body Devices
- Analog and RF Technologies
- SOI Circuit Applications
- Device reliability and characterization
- RFID Technology and Applications
- SOI-specific design

Low-Voltage Microelectronics

Ultra-low-power microelectronics will expand the technological capability of handheld and wireless devices by dramatically improving battery life and portability. Ubiquitous sensor networks, RFID tags, implanted medical devices, portable biosensors, handheld devices, and space-based applications are among those that would benefit from extremely low power circuits. The most efficient way to reduce power is to reduce operating voltage, which can result in energy savings of more than 90% compared to conventional low-power microelectronics. Papers are solicited in the following technical focus areas, but research or concepts in any area of low-voltage microelectronics will be considered:

- Unattended Remote Sensors
- Space-Based Sensors
- Biomedical Devices
- Low-Voltage Handheld/wireless systems
- Ultra-Low-Power Digital Computation
- Analog and RF Technologies
- Energy Management Circuits
- Low Voltage Memory Technologies
- Radiation Effects
- Transistor Variability and Mitigation
- Energy Harvesting Techniques
- Asynchronous Circuits
- Novel Device and Fabrication Technology
- Robust Circuit Design

3D Integration

3D Integration, including monolithic 3D IC or sequential 3D IC, allows us to scale integrated circuits "orthogonally" in addition to classical 2D device and interconnect scaling. This session will address the unique features of such stacking with special emphasis on wafer level bonding as a reliable and cost effective method, similar to the creation of SOI wafers. We will cover fabrication techniques, bonding methods as well as design and test methodologies. Novel inter-strata interconnect schemes will also be discussed. Previously unpublished papers are solicited in all of the above areas related to 3D implementation including:

- Low Thermal Budget Processing
- Processes for Multi Wafer Stacking
- 3D IC EDA and Design Technology
- Fault Tolerant 3D Designs
- Integration of heterogeneous substrates, devices, and architectures
- 3D Manufacturing and Logistics
- Reliability of 3D Circuits
- Cost Analysis of 3D Architectures

DEADLINE INFORMATION

Papers should be submitted no later than April 15, 2016.

Notice of acceptance will be forwarded by June 1st, 2016.

For further information, please visit our website at www.s3sconference.org or contact the conference manager:

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