2015 IEEE S3S Conference Call for Papers

# 2015

IEEE International
SOI-3D-Subthreshold Microelectronics Technology Unified Conference
5 - 8 October 2015
Rohnert Park, California - Sonoma Wine Country

**Welcome to the IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (IEEE S3S)**

Now in its 3rd year as a combined event, the 2015 IEEE S3S Conference will take place in Sonoma Valley, CA, just north of San Francisco. This industry-wide event will gather together widely known experts, contributed papers and invited talks on 3 main topics: SOI technology, subthreshold architectures with associated designs and 3D integration. Combining those three topics enables us to provide extensive and high quality technical content, and makes the conference the perfect venue to present and learn about the most up to date trends in CMOS and post-CMOS Scaling and the low-power SOC eco-system.

The IEEE S3S organizers are pleased to welcome you to this exciting event, which allows attendees to access essentially three conferences with one registration fee.

This year our conference will host parallel tracks for SOI Technology and Subthreshold Microelectronics, complemented by two short courses and two fundamentals classes. In addition, we will feature 3D Integration by having a joint technical session exclusively dedicated to this topic as well as a short course detailing the basics and latest trends in this exciting field.

The usual Hot Topics, Rump and Poster sessions will of course be part of the program, as well as the social events tailored to give much appreciated networking and discussions opportunities. While extended content is made available, we will continue to be the world's premier conference to present and discuss state of the art SOI technical papers.

The conference committee hopes you will enjoy the conference and will actively participate by submitting high quality papers from your organizations.

## SUBMISSION INFORMATION

Prospective authors should prepare a 2-page abstract of their original work including illustrations and indicate a preference for poster or oral presentation. Guidelines for abstract can be found on our website at:
**http://s3sconference.org**

Submissions will be accepted for review in PDF format only and should be e-mailed to: **papers@s3sconference.org**

**Deadline for submissions is April 15, 2015**

## EXECUTIVE COMMITTEE

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|---|---|---|
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## Papers in the following areas are requested

### Silicon On Insulator (SOI)

Ever increasing demand and advances in SOI and related technologies make it essential to meet and discuss new gains and accomplishments in the field. For over 35 years our conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-On-Insulators technology. Previously unpublished papers are solicited in all areas of SOI technology and related devices, circuits and applications, including:

- SOI Device Physics and Modeling
- High-Voltage Devices
- New Devices / Physics Using Advanced Substrates
- SOI Photonics
- New SOI Structures, Circuits and Applications
- Asynchronous Circuits
- Substrate Engineering
- Fully-Depleted / Thin-Body Devices
- Analog and RF Technologies
- SOI Circuit Applications
- SOI Reliability Issues
- Advanced Materials Integration
- SOI Sensors, NEMS, MEMS and RFID Technology and Applications
- Manufacturability and Process Integration of SOI & Fully-Depleted Devices

### Subthreshold Microelectronics

Ultra-low-power microelectronics will expand the technological capability of handheld and wireless devices by dramatically improving battery life and portability. Ubiquitous sensor networks, RFID tags, implanted medical devices, portable biosensors, handheld devices, and space-based applications are among those that would benefit from extremely low power circuits. One of the most promising methods of achieving ultra-low-power microelectronics is to reduce the operating voltage to below the transistor threshold voltage, which can result in energy savings of more than 90% compared to conventional low-power microelectronics. Papers are solicited in the following technical focus areas, but research or concepts in any subject of ultra-low-power microelectronics will be considered.

- Unattended Remote Sensors
- Space-Based Sensors
- Implantable or Wearable Biomedical Devices
- Handheld Biomedical Devices
- Ultra-Low-Power Computation
- Analog and RF Technologies
- Energy Management Circuits
- Memory Technologies
- Radiation Effects
- Transistor Variability and Mitigation
- Energy Harvesting Techniques
- Asynchronous Circuits
- Device and Fabrication Technology
- Robust Circuit Design

### 3D Integration

3D Integration, including monolithic 3D IC or sequantial 3D IC, allows us to scale Integrated circuits “orthogonally” in addition to classical 2D device and interconnect scaling. This session will address the unique features of such stacking with special emphasis on wafer level bonding as a reliable and cost effective method, similar to the creation of SOI wafers. We will cover fabrication techniques, bonding methods as well as design and test methodologies. Novel inter-strata interconnect schemes will also be discussed. Previously unpublished papers are solicited in all of the above areas related to 3D implementation including:

- Manufacturing and Logistics
- Cost Analysis
- Fault Tolerant 3D
- Reliability
- Processing technique adhering to the thermal budget constrains
- Processing advantages and Schemes for Multi Wafer Stacking
- 3D IC EDA and Design Technology
- Hetrogeneous Integration, substrates, functions (logic, memories, linear, RF, electro-optics), architectures

**DEADLINE INFORMATION**

**Papers should be submitted no later than 15 April, 2015.**

Notice of acceptance will be forwarded by 07 June, 2015.

For further information, please visit our website at www.s3sconference.org or contact the conference manager: Joyce Lloyd • 6930 De Celis Pl., #36 • Van Nuys, CA 91406

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